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9 FET Biasing

Unit-2

43194

Introduction

Unlike bipolar transistors, thermal runaway does not occur with field effect transistors. However, the wide differences in maximum and minimum transfer characteristics make I_D levels unpredictable with simple fixed-gate bias voltages. To obtain reasonable limits on quiescent drain currents and drain–source voltages, source resistor and potential divider bias techniques must be employed. For both analysis and design of FET bias circuits, a graphical approach is most convenient. With few exceptions, MOSFET bias circuits are similar to those used for JFETs.

9-1 Dc Load Line and Bias Point

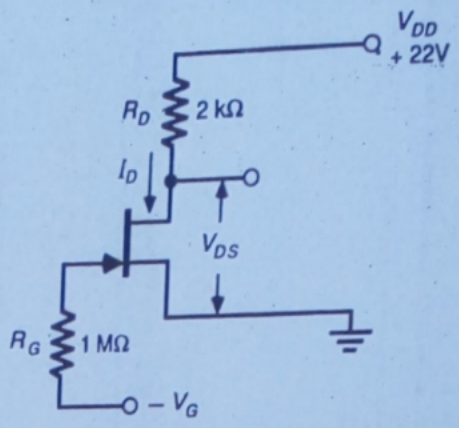
DC Load Line

The dc load line for a field effect transistor circuit is drawn upon the device output characteristics in exactly the same way as for a bipolar transistor circuit (see Section 4-1). Consider the FET circuit and characteristics illustrated in Fig. 9-1. The drain–source voltage V_{DS} is given by

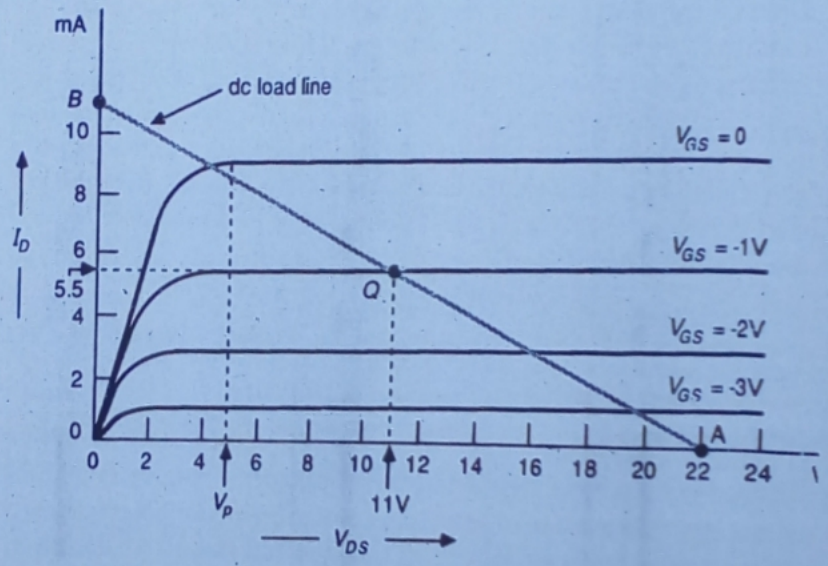
$$V_{DS} = V_{DD} - I_D R_D \tag{9-1}$$

where V_{DD} is the supply voltage and $I_D R_D$ is the voltage drop across R_D. By substituting convenient values of I_D into Eq. 9-1, corresponding levels of V_{DS} can be calculated. These points are then plotted on the characteristics, and the dc load line is drawn through them.

As in the case of bipolar transistor circuits, the dc load line for a FET circuit is a graph of corresponding levels of I_D and V_{DS}. The load line defines all dc values of I_D and V_{DS} that can exist in the circuit. If either V_{DD} or R_D is changed, a new dc load line must be drawn.



(a) Common source circuit using fixed voltage bias



(b) Plotting dc load line

Figure 9-1 The dc load line for a FET circuit can be drawn by plotting any two points. At point *A*, $I_D = 0$ and $V_{DS} = V_{DD}$. At point *B*, $V_{DS} = 0$ and $I_D = V_{DD}/R_D$.

Example 9-1 Using the drain characteristics in Fig. 9-1(b), construct the dc load line for the FET circuit illustrated in Fig. 9-1(a).

Solution

V_{DS} is given by Eq. 9-1,

$$V_{DS} = V_{DD} - I_D R_D$$

When $I_D = 0$,

$$V_{DS} = V_{DD} = 22 \text{ V}$$

Thus, plot point A on the characteristics at

$$V_{DS} = 22 \text{ V and } I_D = 0$$

When $V_{DS} = 0$,

$$0 = V_{DD} - I_D R_D$$

$$I_D = \frac{V_{DD}}{R_D} = \frac{22 \text{ V}}{2 \text{ k}\Omega} = 11 \text{ mA}$$

Hence, plot point B on the characteristics at

$$V_{DS} = 0 \text{ V and } I_D = 11 \text{ mA}$$

Draw the dc load line through points A and B.

Bias Point

A *dc bias point* or *quiescent point* (Q-point) is selected on the FET dc load line. This point defines the dc conditions that exist in a circuit when no input signal is applied. As explained in Section 4-1, the bias point might be selected to give maximum possible changes in output (drain–source) voltage when the drain current is altered by an input signal. In this case the positive-going and negative-going output voltage swings should be as closely equal as possible. Where maximum output voltage swing is not required, the bias point may be at any convenient position on the load line. For the load line in Fig. 9-1(b), with $V_G = -1$ V the bias conditions are $V_{DS} = 11$ V and $I_D = 5.5$ mA.

For a FET amplifier, V_{DS} must remain in the pinch-off region of the characteristics. This means that it must not be allowed to fall below the level of the pinch-off voltage (V_P in Fig. 9-1). Therefore, when designing a FET bias circuit, the drain–source voltage should always be a minimum of (pinch-off voltage) + 1 V:

$$V_{DS(\text{min})} = V_P + 1 \text{ V} \tag{9-2}$$

Where an external bias voltage V_{GS} is included, the pinch-off voltage for that bias level on the drain characteristics is $V_P - V_{GS}$, where V_P is the pinch-off voltage at $V_{GS} = 0$ (see Fig. 8-5). Consequently, the minimum drain–source voltage may be reduced to

$$V_{DS(\text{min})} = V_P - V_{GS} + 1 \text{ V} \tag{9-3}$$

When a FET is used as a switch, the device will either be biased *off* or *on* into the channel ohmic region of the drain characteristics.

9-2 Fixed Voltage Bias Circuit

For a given FET type, typical values of I_{DSS} and V_P are listed on the device data sheet. These quantities cannot be specified to a close tolerance, so, as discussed in Section 8-4, maximum and minimum values are also stated. The maximum and minimum values of I_{DSS} and V_P may easily range to ±50% (or more) of the typical values. Figure 8-10 illustrates the effect of the spread in parameter values upon the transfer characteristics of a 2N5459 FET. A FET with this type number might have the maximum transfer characteristic illustrated, or the minimum characteristic, or a characteristic anywhere between the maximum and minimum.

Consider the circuit in Fig. 9-1(a) once again. The gate of the FET is connected via resistor R_G to a bias voltage $-V_G$. The gate voltage controls the level of drain current in this circuit; nothing else affects I_D. The gate voltage is a fixed quantity, so the circuit is classified as a *fixed voltage bias circuit.* Suppose the minimum transfer characteristic were used in designing the circuit, and suppose further that a FET having the maximum transfer characteristic (or something between the maximum and minimum) were connected into the circuit. Then I_D would be much larger than intended, and the voltage drop across R_D would be larger than the value for which the circuit was designed. Consequently, since $V_{DS} = V_{DD} - I_D R_D$, the drain–source voltage might be so small that the device would be operating in the channel ohmic region of the drain characteristics instead of the pinch-off region [see Fig. 8-5(b)]. If this occurs, the circuit will not function as an amplifier.

The *maximum* transfer characteristics should always be used in FET bias circuit designs. Then the drain current cannot be larger than the design value, and the FET will not be driven into the channel ohmic region of the characteristics. If the FET used in the circuit has a transfer characteristic between the maximum and minimum, I_D will be less than the design level, $I_D R_D$ will be smaller than the value for which the circuit was designed, and V_{DS} will be greater than the required minimum.

For design or analysis of FET bias circuits, a graphical technique using the maximum and minimum transfer characteristics is the most convenient approach. To analyze a fixed voltage bias circuit, a *bias line* is drawn vertically on the transfer characteristics from $V_{GS} = V_G$. The drain current extremes, $I_{D(\max)}$ and $I_{D(\min)}$, are read from the points at which the bias line intersects the maximum and minimum characteristics (see Fig. 9-2). Then $V_{DS(\max)}$ and $V_{DS(\min)}$ are calculated using Eq. (9-1).

As discussed in Section 8-4, a field effect transistor has a very high input resistance. To take advantage of it, R_G should be as large as possible so that the circuit input resistance remains high. However, there is an upper limit to the resistance value that should be used. If R_G is extremely large, a charge accumulated on the gate might take a relatively long time to *leak off.* Thus, the gate voltage would not be a stable quantity, and consequently, the drain

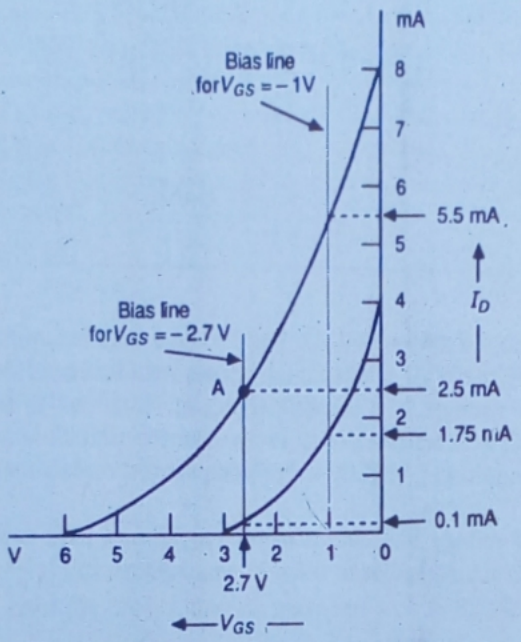


Figure 9-2 Bias lines drawn on the transfer characteristics for fixed voltage bias circuits show the maximum and minimum levels of drain current that might flow in the FET.

current would be unpredictable. A reasonable upper limit is 1 MΩ. Normally R_G should not exceed this value.

Example 9-2

The transfer characteristics for a FET in the fixed bias circuit in Fig. 9-1(a) are shown in Fig. 9-2. If $V_G = -1$ V, determine the maximum and minimum levels of I_D and the corresponding V_{DS} levels.

Solution

$$V_{GS} = V_G = -1 \text{ V}$$

Draw the bias line for $V_G = -1$ V vertically from $V_{GS} = -1$ V, as illustrated in Fig. 9-2. Then, from the points at which the bias line intersects the characteristics,

$$I_{D(\max)} = 5.5 \text{ mA} \quad \text{and} \quad I_{D(\min)} = 1.75 \text{ mA}$$

Using Eq. 9-1,

$$V_{DS} = V_{DD} - I_D R_D$$

so that, for $I_{D(max)}$,

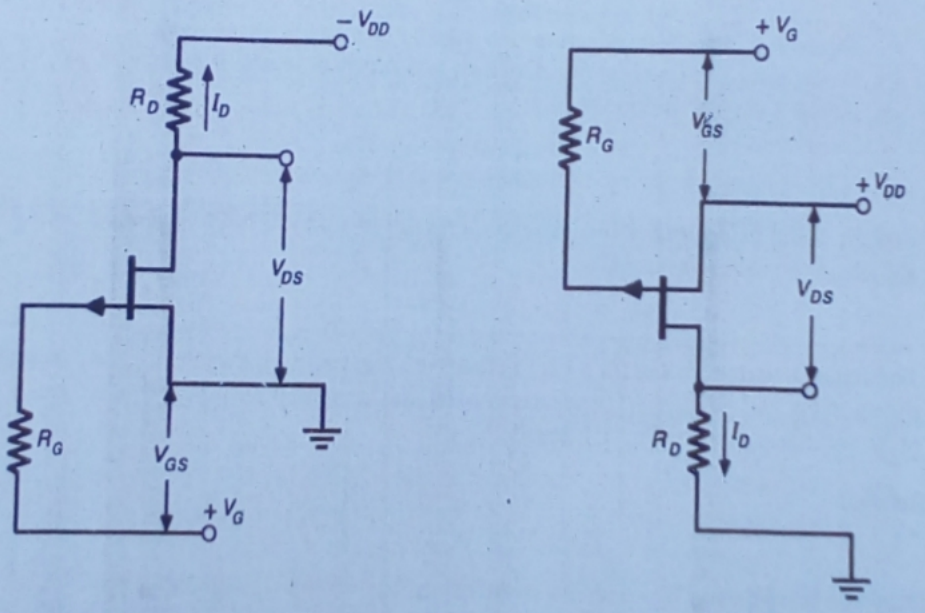
$$V_{DS} = 22\ \text{V} - (5.5\ \text{mA} \times 2\ \text{k}\Omega)$$
$$= 11\ \text{V}$$

and for $I_{D(min)}$,

$$V_{DS} = 22\ \text{V} - (1.75\ \text{mA} \times 2\ \text{k}\Omega)$$
$$= 18.5\ \text{V}$$

Example 9-2 shows that the fixed voltage bias technique is by no means a satisfactory method of obtaining predictable levels of drain current and drain–source voltage. It is possible to adjust V_G to set V_{DS} to a desired level. However, this is acceptable only in an experimental situation. For more reliable bias conditions, slightly more complicated circuit techniques must be employed.

A fixed voltage bias circuit using a *p*-channel FET is illustrated in Fig. 9-3(a). The circuit is similar to the *n*-channel circuit in Fig. 9-1(a), except that



(a) P-channel FET circuit using a $-V_{DD}$ supply.

(b) P-channel FET circuit using a $+V_{DD}$ supply.

Figure 9-3 Fixed voltage bias circuits using *p*-channel FETs. When V_{DD} is negative, V_G must be positive. If a positive V_{DD} is connected to the source, gate bias V_G must be more positive than the source terminal.

V_G is a positive voltage and V_{DD} is negative. Figure 9-3(b) shows the same p-channel circuit with a positive supply. In this case, the FET source terminal is connected to V_{DD}, and R_D is grounded. To reverse bias the gate–channel junction, the gate terminal must be positive with respect to the source. Therefore, gate bias voltage V_G must be positive with respect to V_{DD}.

If the FET in Example 9-2 had been a p-channel device instead of an n-channel one, the calculations would be exactly the same. The only difference would be in the transfer characteristics where V_{GS} would be positive instead of negative.

Example 9-3

Design the fixed bias circuit in Fig. 9-3(a) to have a maximum drain current of 2.5 mA and a minimum drain–source voltage of 8 V. The supply is $V_{DD} = -24$ V, and the FET transfer characteristics are similar to those in Fig. 9-2, except that all V_{GS} levels are positive for a p-channel FET.

Solution

Mark $I_{D(max)}$ at 2.5 mA on the maximum transfer characteristic (point A). From point A, read the corresponding gate–source bias voltage:

$$V_{GS} \approx 2.7 \text{ V}$$

For the fixed bias circuit,

$$V_G = V_{GS} \approx 2.7 \text{ V}$$

From Eq. 8-1,

$$R_D = \frac{V_{DD} - V_{DS}}{I_D}$$

$$= \frac{24 \text{ V} - 8 \text{ V}}{2.5 \text{ mA}} = 6.4 \text{ k}\Omega \quad \text{(use 5.6 k}\Omega \text{ standard value)}$$

$$R_G = 1 \text{ M}\Omega \text{ typically (see text)}$$

Example 9-4

Analyze the fixed voltage bias circuit designed in Example 9-3 to determine $I_{D(min)}$, $V_{DS(max)}$, and $V_{DS(min)}$.

Solution

Draw the vertical bias line for $V_{GS} = 2.7$ V (Fig. 9-2). Where the bias line intersects the minimum transfer characteristic, read

$$I_{D(min)} \approx 0.1 \text{ mA}, \; I_{D(max)} \approx 2.5 \text{ mA}$$

From Eq. 8-1,

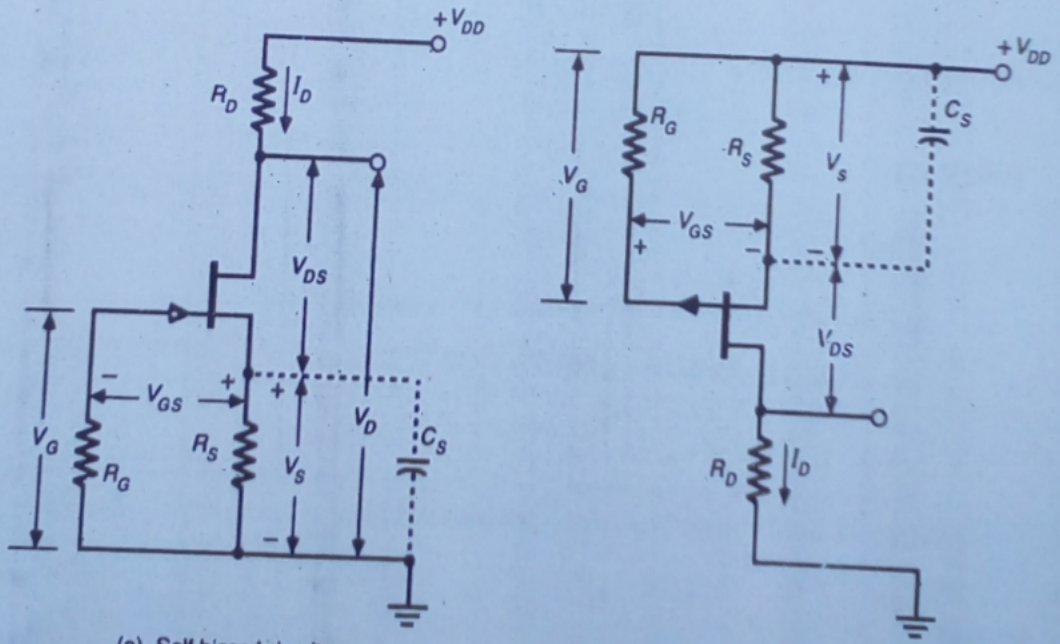
$$V_{DS(max)} = V_{DD} - I_{D(min)}R_D$$
$$= 24\ \text{V} - (0.1\ \text{mA} \times 5.6\ \text{k}\Omega)$$
$$\approx 23.4\ \text{V}$$

$$V_{DS(min)} = V_{DD} - I_{D(max)}R_D$$
$$= 24\ \text{V} - (2.5\ \text{mA} \times 5.6\ \text{k}\Omega)$$
$$= 10\ \text{V}$$

9-3 Self-Bias Circuit

In the *self-bias* circuit, a resistor in series with the FET source terminal provides the gate bias voltage. Consider the *n*-channel FET self-biased circuit shown in Fig. 9-4(a). The voltage drop across R_S is

$$V_S = I_D \times R_S$$



(a) Self biased circuit using *n*-channel FET.

(b) Self biased circuit using *p*-channel FET.

Figure 9-4 Self-biased circuits using *n*-channel and *p*-channel FETs. The voltage drop V_S across source resistor R_S provides the gate–source reverse bias in each case. ($V_{GS} = I_D \times R_S$)

If $I_D = 1$ mA and $R_S = 1$ kΩ, then

$$V_S = 1 \text{ mA} \times 1 \text{ k}\Omega = 1 \text{ V}$$

In this case, the source terminal [in Fig. 9-4(a)] is 1 V positive with respect to ground. Or, alternatively, ground is 1 V negative with respect to the source terminal. Since the FET gate is grounded via R_G, the gate is 1 V negative with respect to the source; i.e., the gate–source bias voltage is $V_{GS} = -1$ V.

In the *p*-channel FET self-bias circuit in Fig. 9-4(b), V_S is again equal to $I_D \times R_S$. But here, V_S makes the FET source terminal 1 V negative with respect to the supply voltage V_{DD}. Consequently, V_{DD} and the FET gate (connected via R_G to V_{DD}) are 1 V positive with respect to the source; i.e., $V_{GS} = +1$ V.

For a FET self-bias circuit,

$$V_{GS} = I_D \times R_S \tag{9-4}$$

Once again, a graphical technique is best for design and analysis of this type of bias circuit, as for all FET bias circuits. As explained in Section 9-2, design calculations should always be made using the maximum transfer characteristic. Drain current I_D is marked on the characteristic, and the required V_{GS} level is read from the horizontal scale. Equation (9-4) is then used to calculate the value of R_S.

For analyzing a self-bias circuit, a bias line is drawn on the transfer characteristics. This bias line is quite different from that for a fixed voltage bias circuit. By inserting R_S and convenient levels of I_D into Eq. (9-4), V_{GS} levels are determined. These corresponding V_{GS} and I_D levels are plotted on the transfer characteristics (see Fig. 9-5), and the bias line is drawn through them. The points where the bias line intersects the transfer characteristics gives $I_{D(\text{max})}$ and $I_{D(\text{min})}$.

Summing the voltage drops across R_D, the FET drain–source terminals and R_S, gives

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S \tag{9-5}$$

Equation (9-5) may be used to calculate the maximum and minimum levels of V_{DS} once $I_{D(\text{max})}$ and $I_{D(\text{min})}$ are determined.

Example 9-5

Design the self-bias FET circuit in Fig. 9-4(a) to have $I_{D(\text{max})} = 2.5$ mA and $V_{DS(\text{min})} = 8$ V. The supply is $V_{DD} = 24$ V, and the FET transfer characteristics are similar to those in Fig. 9-5.

Solution

Mark $I_{D(\text{max})}$ at 2.5 mA on the maximum transfer characteristic (point *A* in Fig. 9-5). When $I_D = 0$,

$$V_{GS} = I_D R_S = 0$$

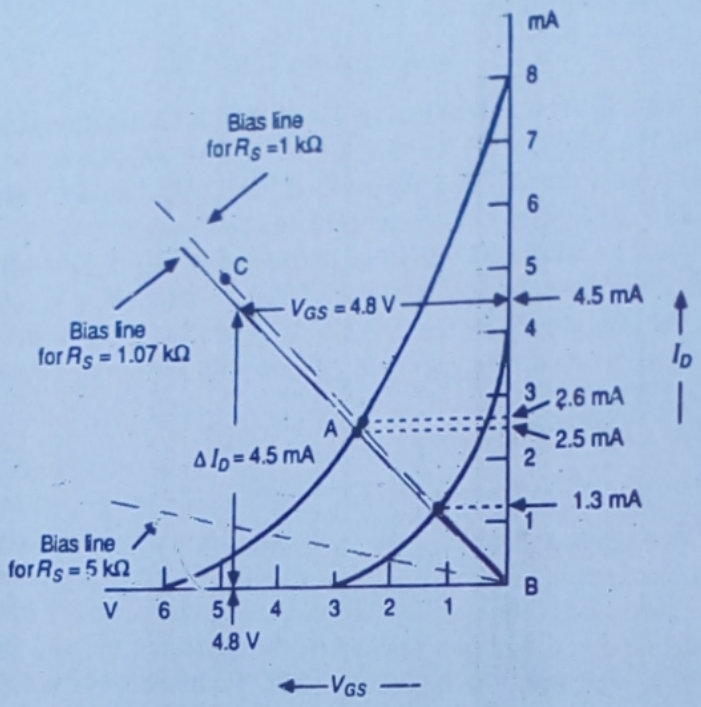


Figure 9-5 The bias line for a self-biased FET circuit is drawn by inserting the value of R_S and convenient levels of I_D into Eq. (9-4), ($V_{GS} = I_D \times R_S$). Corresponding levels of I_D and V_{GS} are then plotted, and the bias line is drawn through them.

Plot point B on the characteristic at $V_{GS} = 0$, $I_D = 0$

Draw the bias line through points A and B. Then

$$R_S = \frac{\Delta V_{GS}}{\Delta I_D} = \frac{4.8\text{ V}}{4.5\text{ mA}} = 1.07\ \Omega \quad \text{(use a 1 k}\Omega\text{ standard resistor)}$$

At $I_{D(max)} = 2.5$ mA,

$$V_{GS} = 2.5\text{ mA} \times 1\text{ k}\Omega$$
$$= 2.5\text{ V}$$

and $$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

or $$I_D R_D = V_{DD} - V_{DS} - I_D R_S$$
$$= 24\text{ V} - 8\text{ V} - 2.5\text{ V}$$
$$= 13.5\text{ V}$$

So $$R_D = \frac{I_D R_D}{I_D} = \frac{13.5\text{ V}}{2.5\text{ mA}}$$
$$= 5.4\text{ k}\Omega \quad \text{(use 4.7 k}\Omega\text{ standard value)}$$

Example 9-6

Analyze the self-biased FET circuit designed in Example 9-5 to determine $I_{D(max)}$, $I_{D(min)}$, $V_{D(max)}$, $V_{D(min)}$, $V_{S(max)}$, $V_{S(min)}$, $V_{DS(max)}$, and $V_{DS(min)}$.

Solution

Since $R_S = 1\ \text{k}\Omega$ instead of the 1.07 kΩ obtained from the bias line, a new bias line for $R_S = 1\ \text{k}\Omega$ should be drawn on the characteristics.

Thus, when $I_D = 0$,

$$V_{GS} = I_D R_S = 0$$

Point B is one point on the bias line for $R_S = 1\ \text{k}\Omega$.

When $I_D = 5\ \text{mA}$,

$$V_{GS} = I_D R_S = 5\ \text{mA} \times 1\ \text{k}\Omega$$
$$= 5\ \text{V}$$

Plot point C on the characteristic at

$$V_{GS} = 5\ \text{V},\ I_D = 5\ \text{mA}$$

Draw the bias line for $R_S = 1\ \text{k}\Omega$ through points B and C in Fig. 9-5. Then, where the bias line for $R_S = 1\ \text{k}\Omega$ intersects the maximum and minimum transfer characteristics, read:

$$I_{D(max)} = 2.6\ \text{mA},\ I_{D(min)} = 1.3\ \text{mA}$$

$$V_{S(max)} = I_{D(max)} R_S$$
$$= 2.6\ \text{mA} \times 1\ \text{k}\Omega = 2.6\ \text{V}$$

$$V_{S(min)} = I_{D(min)} R_S$$
$$= 1.3\ \text{mA} \times 1\ \text{k}\Omega = 1.3\ \text{V}$$

$$V_D = V_{DD} - I_D R_D$$

$$V_{D(max)} = V_{DD} - I_{D(min)} R_D$$
$$= 24\ \text{V} - (1.3\ \text{mA} \times 4.7\ \text{k}\Omega)$$
$$\approx 17.9\ \text{V}$$

$$V_{D(min)} = V_{DD} - I_{D(max)} R_D$$
$$= 24\ \text{V} - (2.6\ \text{mA} \times 4.7\ \text{k}\Omega)$$
$$\approx 11.8\ \text{V}$$

$$V_{DS(max)} = V_{DD} - I_{D(min)} (R_D + R_S)$$
$$= 24\ \text{V} - 1.3\ \text{mA}\ (4.7\ \text{k}\Omega + 1\ \text{k}\Omega)$$
$$\approx 16.6\ \text{V}$$

$$V_{DS(min)} = V_{DD} - I_{D(max)} (R_D + R_S)$$
$$= 24\ \text{V} - 2.6\ \text{mA}\ (4.7\ \text{k}\Omega + 1\ \text{k}\Omega)$$
$$\approx 9.2\ \text{V}$$

Example 9-6 demonstrates that the self-bias technique gives closer limits on I_D, and consequently on V_{DS}, than the fixed voltage bias method. Using larger resistance values for R_S makes $I_{D(max)}$ and $I_{D(min)}$ even closer. However, as shown by the bias line for $R_S = 5\ \text{k}\Omega$ in Fig. 9-5, I_D might be reduced to quite low levels when larger values of R_S are used.

Bypass capacitor C_S is included in each of the circuits in Fig. 9-4. This capacitor performs exactly the same function as the bypass capacitor across the emitter resistor in a BJT emitter current bias circuit (Section 4-8). If C_S were not present, the circuit voltage gain (from gate to drain) would be severely restricted. The total dc load for a self-biased circuit is $R_D + R_S$. The ac load with R_S bypassed (and no capacitor-coupled load) is R_D. Thus, as in for bipolar circuits, separate ac and dc load lines must be drawn to describe the FET circuit performance.

9-4 Potential Divider Bias

For the self-biased circuit in Section 9-3, it was seen that the use of larger values of source resistance R_S bring $I_{D(max)}$ and $I_{D(min)}$ closer together, but lower levels of I_D result from using large R_S values. As will be demonstrated, *potential divider bias* allows the use of reasonably large R_S values without making I_D very small.

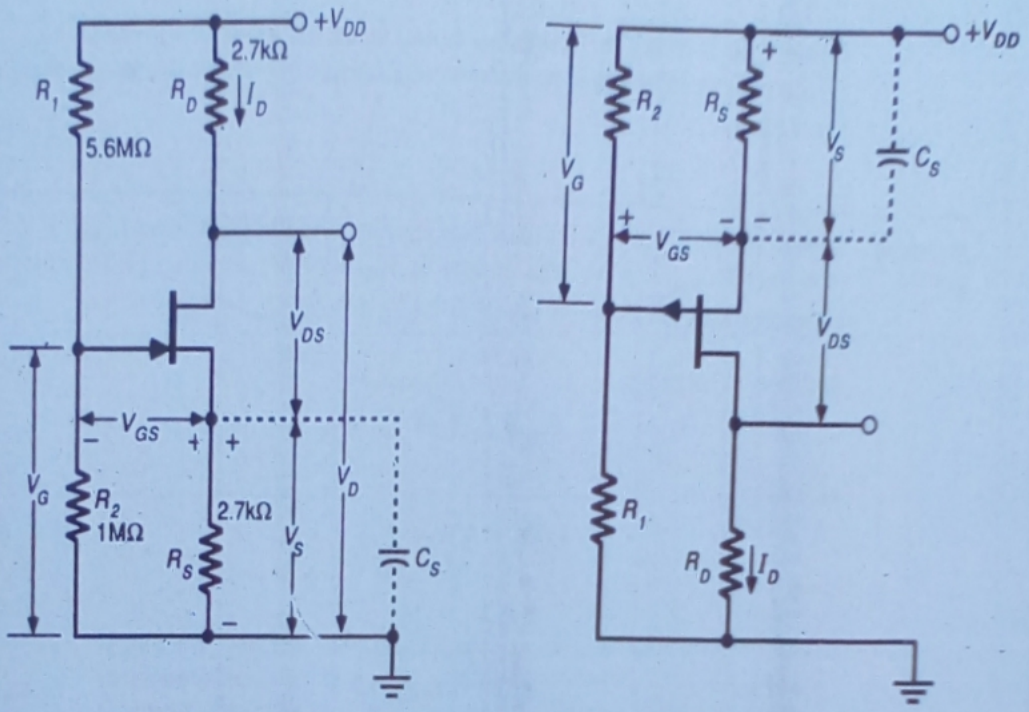
Two FET potential divider bias circuits are illustrated in Fig. 9-6. This type of circuit combines the use of a source resistor, as in the self-bias circuit, with a gate bias voltage V_G derived from the supply voltage by means of a potential divider. Referring to the *n*-channel FET circuit in Fig. 9-6(a), it is seen that V_G makes the gate positive with respect to ground. The voltage drop across R_S, namely, $V_S = I_D R_S$, makes the source terminal positive with respect to ground. V_S is always larger than V_G, so the source terminal is at a higher potential than the gate. Thus, the gate is negative with respect to the source.

In the *p*-channel circuit in Fig. 9-6(b), V_S makes the source terminal negative with respect to V_{DD}. The potential divider voltage V_G makes the gate negative with respect to V_{DD}. Here again, V_S is larger than V_G, thus making the gate positive with respect to the source. This, of course, is the required polarity for reverse gate–source bias on the *p*-channel FET.

Both circuits in Fig. 9-6 employ bypass capacitors across source resistor R_S. This is done to maximize the circuit ac gain, as explained in Section 9-3.

Once again, the graphical technique of drawing a bias line on the FET transfer characteristics is the best method for both design and analysis of the bias circuit. An equation relating V_{GS} and I_D must be derived, so that corresponding values of each quantity may be calculated for plotting the bias line. As discussed above,

$$V_{GS} = V_G - I_D R_S \tag{9-6}$$



(a) Potential divider bias circuit using n-channel FET

(b) Potential divider bias circuit using p-channel FET

Figure 9-6 Potential divider bias circuits for *n*-channel and *p*-channel FETs. Gate bias voltage V_G is always less than the voltage V_S across R_S. This condition produces a reverse bias at the gate–source terminals.

Since there is no gate current,

$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

Therefore,

$$V_{GS} = \frac{V_{DD} \times R_2}{R_1 + R_2} - I_D R_S \qquad (9\text{-}7)$$

As usual, design of the circuit commences with specified levels of V_{DD}, $I_{D(max)}$ and $V_{DS(min)}$. For the potential divider bias circuit, V_S cannot be obtained directly from the transfer characteristic when $I_{D(max)}$ is plotted. Instead, V_{DD} must first be divided between V_{RD}, V_{DS}, and V_S. With $V_{DS(min)}$ specified, the remaining portion of V_{DD} is split between V_{RD} and V_S. As will be shown in Chapter 10, the gain of a FET amplifier stage is directly proportional to R_D. Maximum gain is achieved by making R_D as large as possible, and for a given level of I_D this requires maximum voltage drop across R_D. However, greatest bias stability is achieved by making R_S as large as possible, and this dictates maximum V_S. A reasonable compromise between these two conflicting re-

gain ↗ large R_D ↑stabs – R_S ↗

quirements is to make V_S and V_{RD} equal. Once the value of V_S is decided, all the resistor values may be calculated. Example 9-7 demonstrates the design procedure.

Example 9-7 Design the FET potential divider bias circuit in Fig. 9-6(a) to have $I_{D(max)} = 2.5$ mA and $V_{DS(min)} = 8$ V. The supply is $V_{DD} = 24$ V, and the FET transfer characteristics are those of Fig. 9-7.

Solution

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

or

$$I_D R_D + I_D R_S = V_{DD} - V_{DS}$$
$$= 24 \text{ V} - 8 \text{ V} = 16 \text{ V}$$

Let

$$I_D R_D = I_D R_S = 8 \text{ V}$$

For $I_{D(max)} = 2.5$ mA,

$$R_D = R_S = \frac{8 \text{ V}}{2.5 \text{ mA}}$$
$$= 3.2 \text{ k}\Omega \quad \text{(use 2.7 k}\Omega \text{ standard value)}$$

Mark $I_{D(max)}$ at 2.5 mA on the maximum transfer characteristic (point A on Fig. 9-7). Then for $\Delta I_D = 2.5$ mA,

$$\Delta V_{GS} = \Delta I_D \times R_S$$
$$= 2.5 \text{ mA} \times 2.7 \text{ k}\Omega = 6.75 \text{ V}$$

Mark point B at ΔV_{GS}, ΔI_D from point A (see Fig. 9-7). Then draw the (design) bias line through points A and B. From point B, read

$$V_{R2} = V_G \approx 4.1 \text{ V}$$

Let $R_2 = 1$ MΩ (see Section 9-2). Then

$$I_2 = \frac{V_{R2}}{R_2} = \frac{4.1 \text{ V}}{1 \text{ M}\Omega} = 4.1 \text{ μA}$$

$$V_{R1} = V_{DD} - V_{R2}$$
$$= 2.5 \text{ V} - 4.1 \text{ V} = 20.9 \text{ V}$$

$$R_1 = \frac{V_{R1}}{I_2} = \frac{20.9 \text{ V}}{4.1 \text{ μA}}$$
$$= 5.1 \text{ M}\Omega \quad \text{(use 5.6 M}\Omega \text{ standard value)}$$

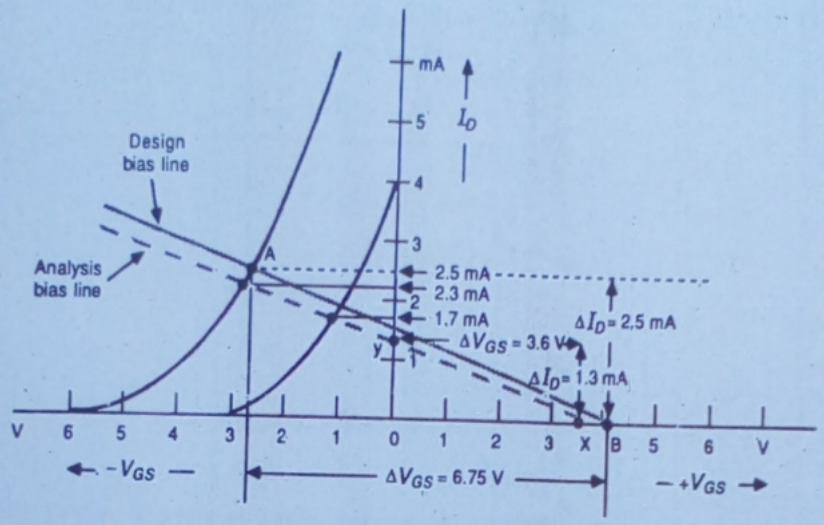


Figure 9-7 The bias line for a FET potential divider bias circuit is drawn by inserting the value of R_S and convenient levels of I_D into Eq. (9-7). Corresponding levels of I_D and V_{GS} are then plotted, and the bias line is drawn through them.

To analyze a FET potential divider bias circuit, Eq. 9-7 is used to plot the bias line. The intersections of the bias line and the transfer characteristics give $I_{D(max)}$ and $I_{D(min)}$. Once these levels are determined, the maximum and minimum voltages throughout the circuit can be readily calculated.

Analyze the circuit designed in Example 9-7 to determine $I_{D(max)}$, $I_{D(min)}$, $V_{D(max)}$, $V_{D(min)}$, $V_{S(max)}$, $V_{S(min)}$, $V_{DS(max)}$, and $V_{DS(min)}$. **Example 9-8**

Solution

$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2} = \frac{24\text{ V} \times 1\text{ M}\Omega}{5.6\text{ M}\Omega + 1\text{ M}\Omega}$$
$$= 3.6\text{ V}$$

Plot point X on the transfer characteristic in Fig. 9-7 at $V_{GS} = 3.6$ V, $I_D = 0$. For $\Delta V_{GS} = 3.6$ V,

$$\Delta I_D = \frac{\Delta V_{GS}}{R_S} = \frac{3.6\text{ V}}{2.7\text{ k}\Omega} = 1.33\text{ mA}$$

Plot point Y at ΔV_{GS} and ΔI_D from point X in Fig. 9-7. Then draw the bias line through points X and Y. From the bias line, read

$$I_{D(max)} \approx 2.3 \text{ mA}, I_{D(min)} \approx 1.7 \text{ mA}$$

$$V_{S(max)} = I_{D(max)} R_S$$
$$= 2.3 \text{ mA} \times 2.7 \text{ k}\Omega \approx 6.2 \text{ V}$$

$$V_{S(min)} = I_{D(min)} R_S$$
$$= 1.7 \text{ mA} \times 2.7 \text{ k}\Omega \approx 4.6 \text{ V}$$

$$V_{D(max)} = V_{DD} - I_{D(min)} R_D$$
$$= 24 \text{ V} - (1.7 \text{ mA} \times 2.7 \text{ k}\Omega)$$
$$\approx 19.4 \text{ V}$$

$$V_{D(min)} = V_{DD} - I_{D(max)} R_D$$
$$= 24 \text{ V} - (2.3 \text{ mA} \times 2.7 \text{ k}\Omega)$$
$$\approx 17.8 \text{ V}$$

$$V_{DS(max)} = V_{DD} - I_{D(min)} (R_D + R_S)$$
$$= 24 \text{ V} - 1.7 \text{ mA} (2.7 \text{ k}\Omega + 2.7 \text{ k}\Omega)$$
$$\approx 14.8 \text{ V}$$

$$V_{DS(min)} = V_{DD} - I_{D(max)} (R_D + R_S)$$
$$= 24 \text{ V} - 2.3 \text{ mA} (2.7 \text{ k}\Omega + 2.7 \text{ k}\Omega)$$
$$\approx 11.6 \text{ V}$$

The results of Example 9-8 show that the $I_{D(max)}$ and $I_{D(min)}$ levels are closer with potential divider bias than with self-bias. In Examples 9-4, 9-6, and 9-8, the three basic types of FET bias circuit are analyzed. All three circuits were designed to meet the same bias specification for $I_{D(max)}$ and $V_{DS(min)}$. It is clear that the potential divider bias circuit provides the most predictable bias conditions. Also, self-bias is not as good as potential divider bias, but is substantially better than fixed voltage bias.

9-5 More JFET Bias Circuits

Drain Feedback Bias

The FET bias circuit in Fig. 9-8 is essentially potential divider bias. However, instead of the supply voltage being potentially divided by R_1 and R_2, the drain voltage V_D is potentially divided to provide the gate bias. This arrangement is similar to the BJT circuits in Fig. 4-11, which combine emitter current bias and collector-to-base bias. The circuit is designed for a particular level of V_D and I_D. When I_D is greater than the design value, there is a larger voltage drop across R_D, and V_D is reduced. The reduction in V_D results in a reduced level

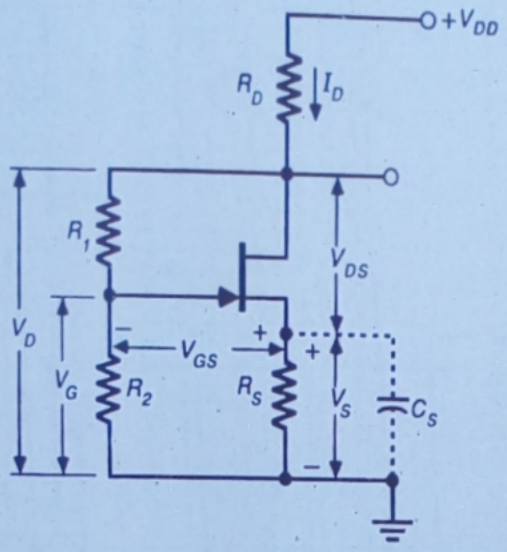


Figure 9-8 The FET drain feedback bias circuit is similar to the potential divider bias circuit, but instead of dividing supply voltage V_{DD}, drain voltage V_D is potentially divided to provide gate bias V_G. This gives a further improvement in bias stability.

of V_G. The increased level of I_D also increases V_S. These two effects (increased V_S and reduced V_G) give a larger gate–source reverse bias voltage V_{GS} and thus tend to push I_D back towards its design level. $I_{D(max)}$ and $I_{D(min)}$ are even closer together with this circuit than with an ordinary potential divider bias circuit.

Design procedure for the circuit in Fig. 9-8 is exactly the same as for the potential divider bias circuits discussed in Section 9-4. The one exception is that the voltage across R_1 is now $V_D - V_{R2}$, instead of $V_{DD} - V_{R2}$. For circuit analysis, a bias line should be drawn, as always. This requires the equation relating V_{GS} and I_D:

$$V_{GS} = \frac{R_2(V_{DD} - I_D R_D)}{R_1 + R_2} - I_D R_S \qquad (9\text{-}8)$$

Source Current Bias

Each FET bias circuit considered so far has improved bias stability by making the bias line flatter than was possible with the previous circuit. Obviously, a flatter bias line minimizes the difference between $I_{D(max)}$ and $I_{D(min)}$. The circuit in Fig. 9-9 gives a horizontal bias line by using a bipolar transistor with emitter current bias to stabilize I_S. Since $I_D = I_S$, the FET drain current remains constant. If the circuit is to be an amplifier, the FET source terminal must be capacitor-bypassed to ground as illustrated, for the reasons already discussed. The transistor emitter circuit does not need a bypass capacitor, since no signal is to be applied to its base.

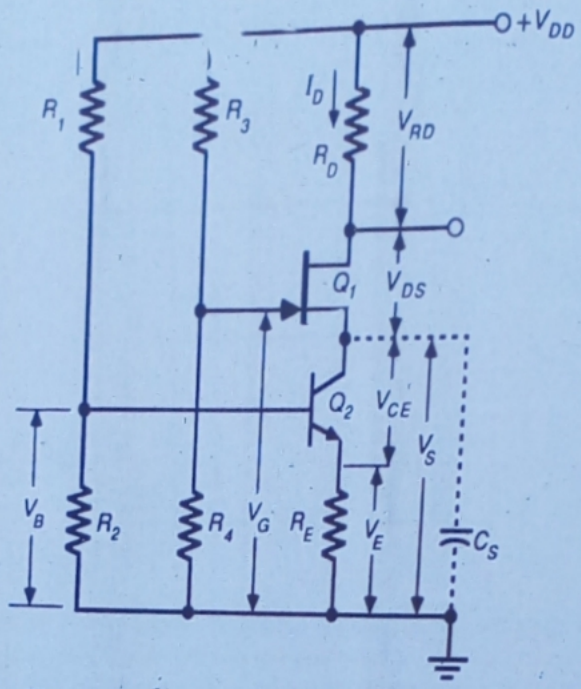


Figure 9-9 The source current bias circuit uses a bipolar transistor with emitter current bias to stabilize the FET drain current at a constant level.

Design of the circuit in Fig. 9-9 simply involves selection of appropriate voltage and current levels and calculation of the resistors. The maximum gate–source reverse bias voltage V_{GS} is first determined by plotting I_D on the maximum transfer characteristic and reading $V_{GS(max)}$ at I_D. Emitter voltage V_E should typically be a minimum of 5 V, but satisfactory emitter current stability can be achieved with as little as 3 V. To avoid transistor saturation, V_{CE} should be approximately ($V_{GS(max)}$ + 2 V). The source voltage V_S equals $V_{CE} + V_E$, as illustrated. V_G is calculated as $V_S - V_{GS(max)}$. The voltage across drain resistor R_D is ($V_{DD} - V_{DS(min)} - V_S$). The FET and bipolar potential divider circuits are designed in the usual way for each device.

Use of ± Supply Voltages

When ± supply voltages are to be used, the FET gate would normally be grounded via a resistor, as illustrated in Fig. 9-10. In this case, the circuit behaves as a potential divider bias circuit with V_G equal to V_{SS}. The voltage at the FET source terminal is $+V_{GS}$ above the level of the grounded gate. This means that the sum of V_{RD} and V_{DS} is ($V_{DD} - V_{GS}$), and the voltage drop across the source resistor is $V_S = V_{GS} + V_{SS}$.

Once the voltage levels are understood, design of the circuit follows essentially the same procedure as used for the potential divider bias circuit. That is, $I_{D(max)}$ is plotted on the maximum transfer characteristics, and V_{GS} is read from the horizontal axis. Then, with I_D and the voltage drops known, R_D and R_S are readily calculated. R_G is selected as 1 MΩ or less, as explained in

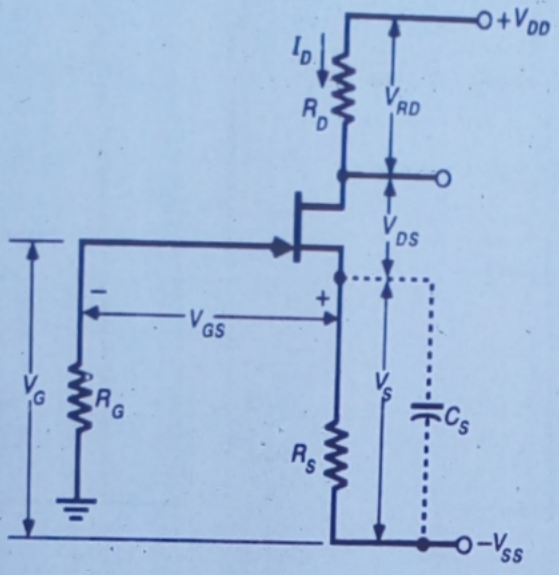


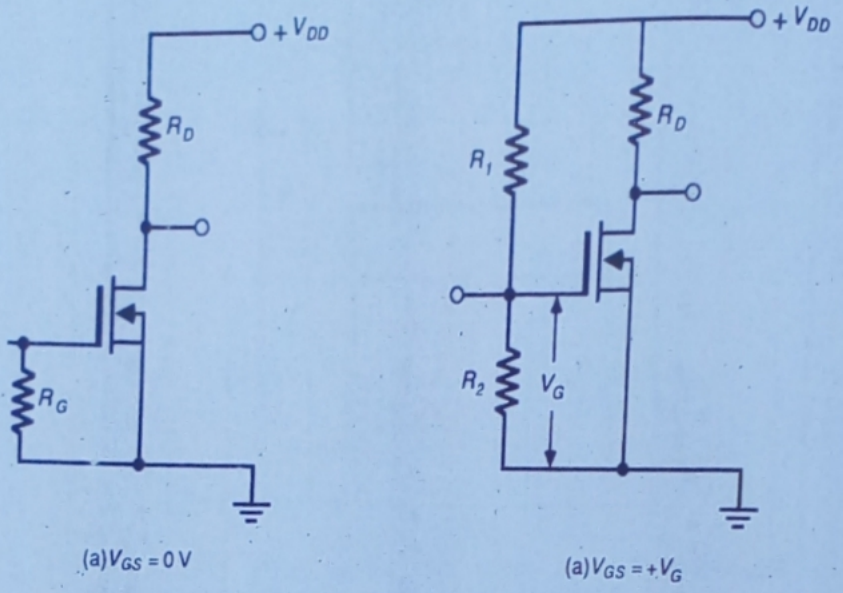
Figure 9-10 Potential divider bias using ± supply voltages. With $V_G = V_{SS}$, this circuit behaves exactly the same as other potential divider bias circuits.

Section 9-2. Analysis for this circuit is exactly as for the potential divider bias circuit.

9-6 Biasing MOSFETs

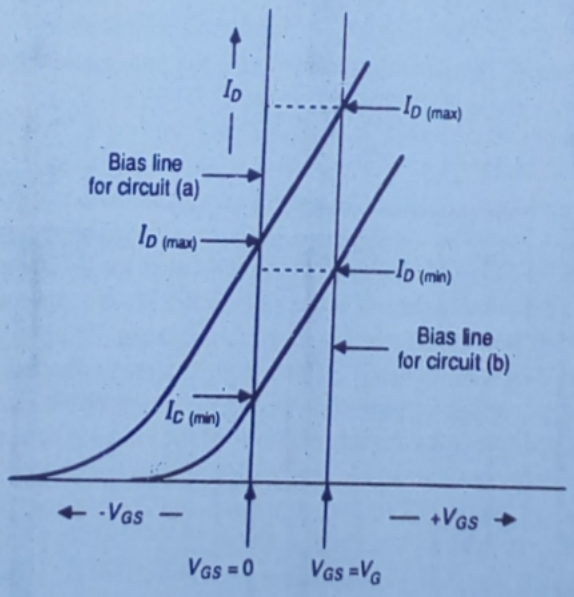
MOSFET bias circuits are quite similar to the circuits used for JFET biasing. In the case of depletion-enhancement types of MOSFETs, the gate–source voltage may be either positive or negative in both *n*-channel and *p*-channel devices (see Section 8-8). Any of the JFET bias circuits already discussed can be used to give a negative V_{GS} for an *n*-channel device, or a positive V_{GS} for a *p*-channel type. To operate an *n*-channel MOSFET in the enhancement mode (either a depletion-enhancement device or a purely enhancement type), the gate must be biased positively with respect to the source. The self-bias circuit is unsuitable in this case, and if fixed voltage bias is to be used, V_{GS} must be a positive quantity. The same remarks apply for a *p*-channel MOSFET operated in the enhancement mode, except that the gate must be negative with respect to the source.

Consider the two fixed voltage bias circuits and the transfer characteristics shown in Fig. 9-11. Each circuit employs a depletion-enhancement FET, so V_{GS} may be positive, negative or zero. In Fig. 9-11(a), the gate terminal is connected to the source via resistor R_G. V_{GS} is zero, and the bias line is drawn on the transfer characteristics at that value of V_{GS}, [Fig. 9-11(c)]. As always, $I_{D(max)}$ and $I_{D(min)}$ are read at the intersection of the bias line and the transfer



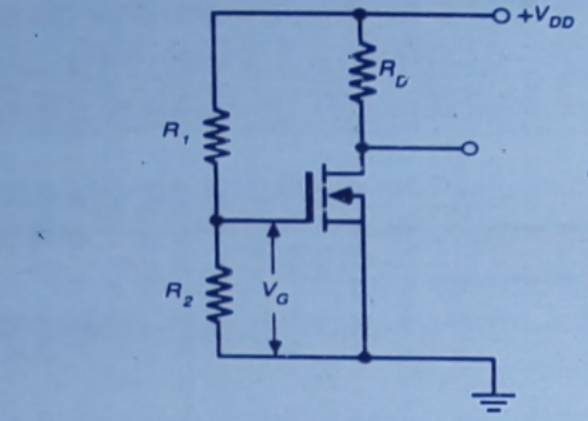
(a) $V_{GS} = 0$ V

(a) $V_{GS} = +V_G$

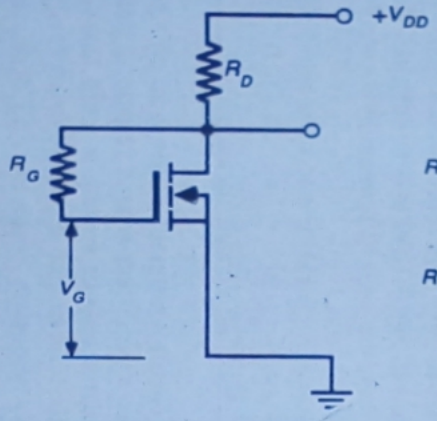


(c) Graphic analysis

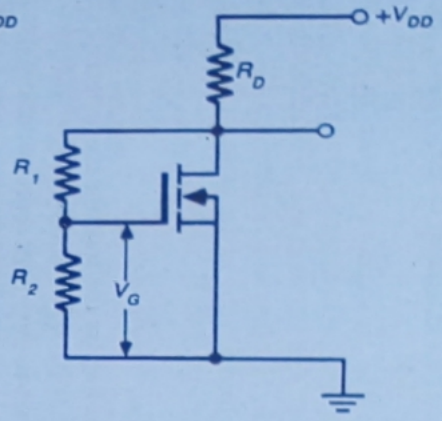
Figure 9-11 Depletion-enhancement MOSFETs may have positive, negative, or zero gate–source voltage. For fixed voltage bias, the bias line is drawn vertically on the transfer characteristics at $V_{GS} = V_G$.



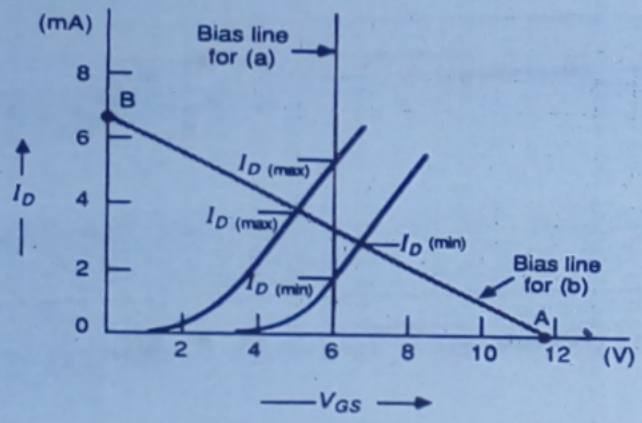
(a) Fixed voltage bias



(b) Drain-to-gate bias



(c) Drain-to-gate bias with a potential divider



(d) Graphic analysis

Figure 9-12 The gate–source bias voltage for *n*-channel enhancement MOSFETs must be positive for a drain current to flow. For circuit (a), $V_G = V_{DD} R_2 / (R_1 + R_2)$. For circuit (b), $V_G = V_D$. For (c), $V_G = V_D R_2 / (R_1 + R_2)$.

characteristics. In the circuit in Fig. 9-11(b), V_G is a positive quantity derived from V_{DD} via R_1 and R_2. As illustrated on the transfer characteristics, the bias line for this circuit is drawn at $V_{GS} = +V_G$.

n-channel enhancement MOSFETs are employed in the circuits shown in Fig. 9-12. These devices must have their gate terminals positive with respect to the source for drain current to flow. The circuit in Fig. 9-12(a) is similar to that in Fig. 9-11(b), and once again the bias line must be drawn at $V_{GS} = +V_G$. In Fig. 9-12(b) the FET gate is connected directly to the drain terminal via R_G (*drain-to-gate* bias). V_G is then always equal to V_D. Also,

$$V_G = V_{DD} - I_D R_D \tag{9-9}$$

Equation 9-9 is used to draw the bias line on the transfer characteristics. At point A, $I_D = 0$ and $V_{GS} = V_{DD}$; at point B, $V_G = 0$ and $I_D = V_{DD}/R_D$.

In situations where a direct drain-to-gate connection would make the drain–source voltage too low, the circuit in Fig. 9-12(c) may be suitable. This is simply a variation of drain-to-gate bias, but with V_D potentially divided by R_1 and R_2.

9-7 Biasing FET Switching Circuits

A field effect transistor in a switching circuit is normally either in an *off* state with zero drain current, or in an *on* state with drain–source voltage as small as possible. As in the case of a bipolar transistor switch, a small leakage current flows when the FET is off. This drain–source leakage current is normally so small that it can be completely neglected. When the FET is on, the minimum drain–source voltage is unlike the saturation voltage that occurs with a bipolar transistor. In an on-biased JFET, there is no depletion region penetration into the channel. Consequently, the voltage drop from drain to source is simply the drain current times the channel resistance:

$$V_{DS(on)} = I_D \times R_{D(on)} \tag{9-10}$$

Some field effect transistors, designed specifically for switching, have very low resistance channels. For example, the 2N4856 JFET has $R_{D(on)} = 25\ \Omega$ (see the data sheet in Appendix 1-10). With low drain current levels, $V_{DS(on)}$ can be much smaller than the 0.2 V that is typical of $V_{CE(sat)}$ with a bipolar transistor.

Figure 9-13(a) shows a direct-coupled JFET switching circuit. When $V_i = 0$, the FET gate and source terminals are at the same potential and there is no depletion region penetration. The output voltage is then $V_o = V_{DS(on)}$, as expressed in Eq. 9-10. To switch the FET off, V_i should exceed the maximum pinch-off voltage for the device. The input amplitude can be larger than V_P, but not so large that $V_{DD} - V_i$, (the total voltage across the drain–gate terminals) approaches the drain–gate breakdown voltage. A rule-of-thumb is to let V_i equal $V_{P(max)} + 1$ V.

Noise Figure

One advantage of a FET over a bipolar transistor is that the FET usually has much lower thermal noise. This is because, unlike the bipolar transistor, there are very few charge carriers crossing a junction in the FET. As in the case of bipolar device, the FET *noise figure NF* is specified as a *spot noise figure* at a particular frequency and bias conditions, and for a given value of bias resistance. The figure varies if any of these conditions are altered. Noise calculations for a FET circuit are performed in the same way as for a bipolar transistor circuit.

Capacitances

Capacitances for FETs may be specified as *gate–drain capacitance* C_{gd}, *gate–source capacitance* C_{gs}, and *drain–source capacitance* C_{ds}. Instead of these, the capacitance is sometimes specified as the *common source input capacitance* C_{iss} or C_{gss}. This is the gate–source capacitance measured with the drain shorted to the source. In this case a *reverse transfer capacitance* C_{rss} is also specified, C_{rss} being another term for C_{gd}. These quantities are very important for FET high-frequency and switching circuits. For the 2N5457, C_{iss} is 7 pF maximum and C_{rss} is 3 pF maximum (Appendix 1-8).

8-5 FET Voltage Amplification

As already explained, the FET is a voltage-operated device. A change in gate–source voltage V_{GS} produces a change in drain current I_D. The change in I_D results in a change in output voltage V_D.

Consider the basic FET circuit shown in Fig. 8-12. Note that the gate–source is reverse biased by dc voltage V_G. A signal generator voltage V_i is included in series with the device gate. The drain is supplied by dc voltage V_{DD}.

Suppose that $V_{DD} = 20$ V, $R_1 = 6$ kΩ, $g_m = 2000$ μS, and V_G is adjusted to give $I_D = 2$ mA. Then, when $V_i = 0$,

$$\begin{aligned} V_D &= V_{DD} - I_D R_1 \\ &= 20 \text{ V} - (2 \text{ mA} \times 6 \text{ k}\Omega) \\ &= 8 \text{ V} \end{aligned}$$

Now assume that the signal generator voltage is increased from zero to $v_i = \pm 50$ mV. This produces a change in I_D given by

$$\begin{aligned} \Delta I_D &= g_m V_i \\ &= 2000 \text{ μS} \times (\pm 50 \text{ mV}) \\ &= \pm 0.1 \text{ mA} \end{aligned}$$

When $\Delta I_D = +0.1$ mA,

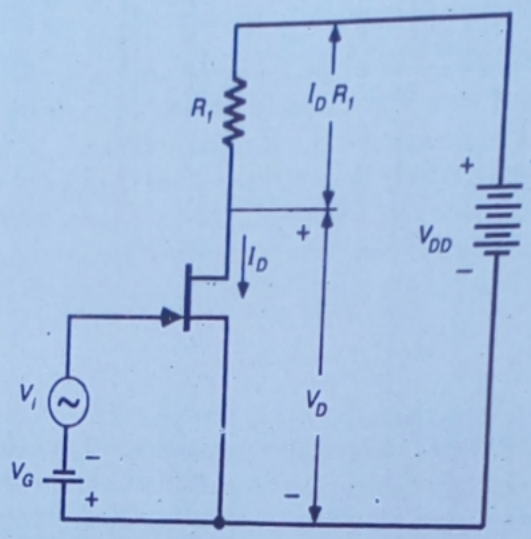


Figure 8-12 When a signal voltage $\pm V_i$ is applied to the gate of a FET, it produces a change in drain current $\pm\Delta I_D$. This change, in turn, alters the voltage drop across R_1, to give a change in (output) drain voltage $\pm\Delta V_D$.

$$\begin{aligned} V_D &= V_{DD} - R_1(I_D + \Delta I_D) \\ &= 20\text{ V} - 6\text{ k}\Omega\ (2\text{ mA} + 0.1\text{ mA}) \\ &= 7.4\text{ V} \end{aligned}$$

Thus, V_D has fallen from 8 V to 7.4 V, or

$$\Delta V_D = -0.6\text{ V}$$

When $\Delta I_D = -0.1$ mA,

$$\begin{aligned} V_D &= 20\text{ V} - 6\text{ k}\Omega(2\text{ mA} - 0.1\text{ mA}) \\ &= 8.6\text{ V} \end{aligned}$$

Hence, V_D has increased from 8 V to 8.6 V, or

$$\Delta V_D = +0.6\text{ V}$$

It is seen, then, that a signal of $v_i = \pm 50$ mV produced an output of $v_o = \pm 0.6$ V. The voltage amplification is

$$\begin{aligned} A_v &= \frac{v_o}{v_i} \\ &= \frac{\pm 0.6\text{ V}}{\pm 50\text{ mV}} \\ &= 12 \end{aligned}$$

8-6 JFET Construction

Junction field effect transistors are normally constructed by the diffusion process (Chapter 6). Figure 8-13 illustrates one type of construction. Starting with a *p*-type substrate, an *n*-channel is diffused. Then *p*-type impurities are diffused into the *n*-channel to form one side of the gate, the substrate forming the other side of the gate. Finally, metal is deposited in place to make terminals. With this symmetrical type of construction, the drain and source are interchangeable. Other fabrication techniques produce devices in which the geometry is not symmetrical. In such cases interchanging the drain and source terminals would radically affect the device characteristics.

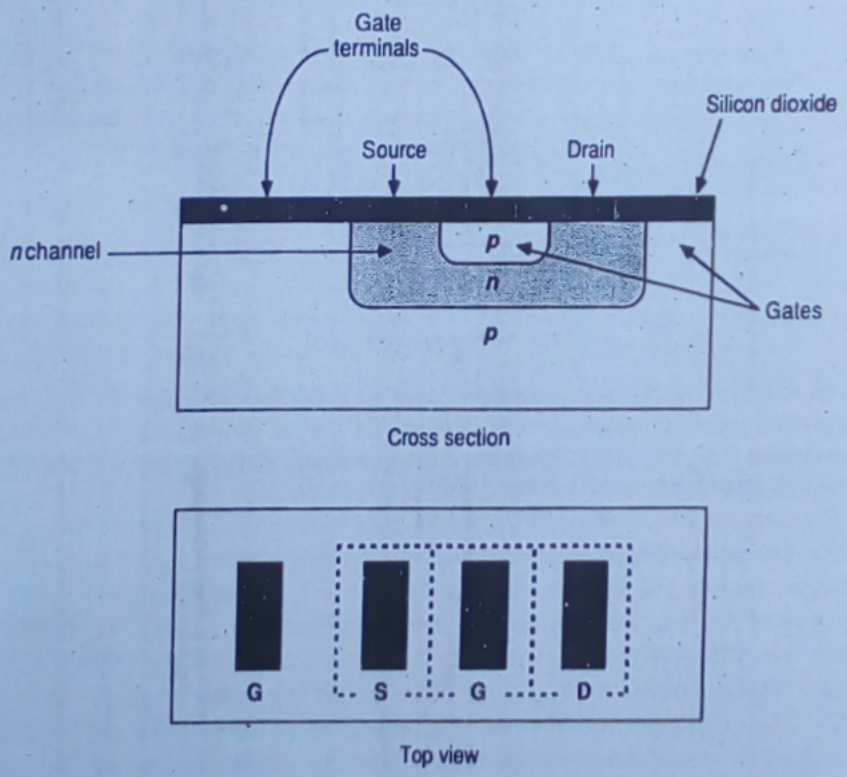
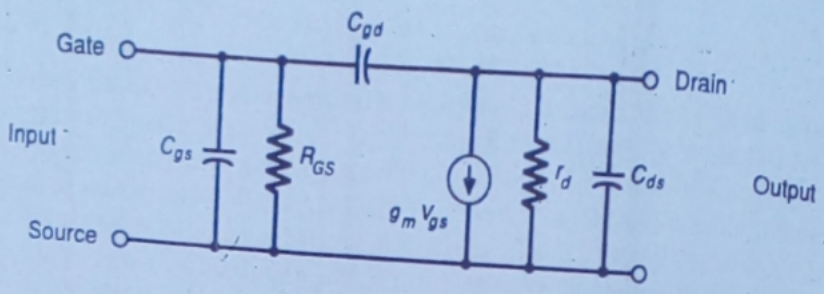


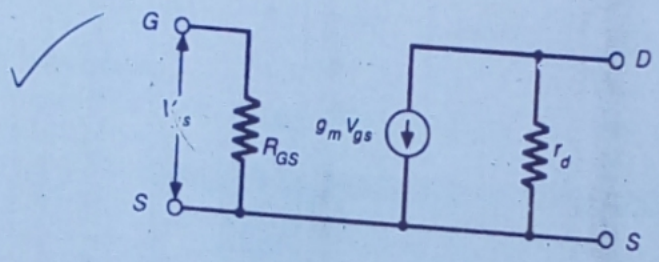
Figure 8-13 Cross section and top view of diffused *n*-channel JFET. In this particular device the drain and source may be interchangeable.

8-7 FET Equivalent Circuit

The complete common source ac equivalent circuit for a field effect transistor is shown in Fig. 8-14(a). The source is common to both input and output



(a) Complete equivalent circuit.



(b) Low frequency ac equivalent circuit

Figure 8-14 The complete equivalent circuit for a junction field effect transistor includes interterminal capacitances, as well as gate–source resistance R_{GS}, drain resistance r_d and current generator $g_m V_{GS}$. In the low-frequency equivalent circuit the capacitances are omitted.

terminals. The output circuit is defined in terms of a current source $g_m \times V_{gs}$ supplying current to a drain resistance r_d. Note that V_{gs} is the ac (signal) voltage applied between gate and source. The drain–source capacitance C_{ds} appears in parallel with the output terminals. Input signals will "see" the gate–source leakage resistance R_{GS} in parallel with the gate–source capacitance C_{gs}. The drain–gate capacitance C_{gd} is shown connected between the drain and gate terminals. For low-frequency operation, the capacitors may be eliminated. The simplified low-frequency equivalent circuit is as shown in Fig. 8-14(b).

8-8 The MOSFET

Enhancement MOSFET

Figure 8-15(a) shows the construction of an *insulated gate FET* or *metal oxide semiconductor FET* (MOSFET). Starting with a high-resistive *p*-type sub-

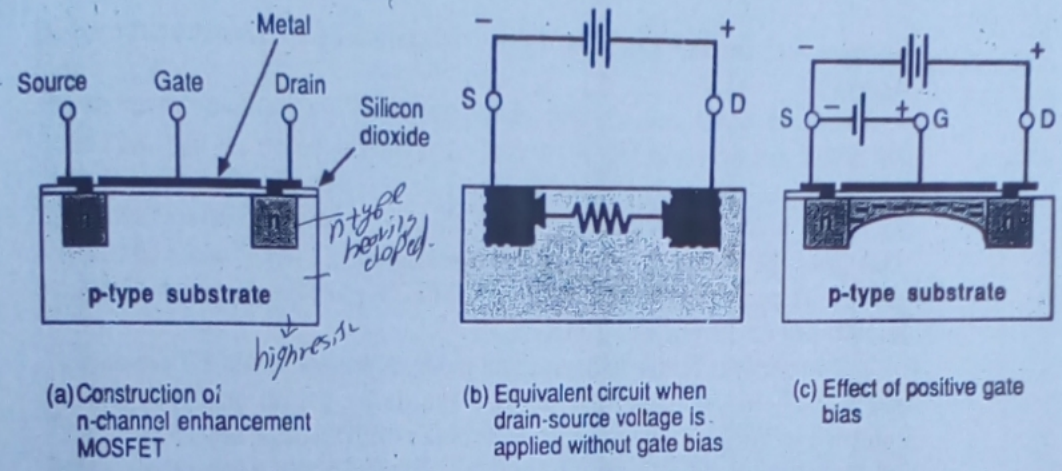


Figure 8-15 In the *n*-channel enhancement MOSFET, no channel exists until the gate is made positive with respect to the substrate. The positive potential on the gate attracts negative charge carriers to form a channel between drain and source terminals.

strate, two blocks of heavily doped *n*-type material are diffused into the substrate, and then the surface is coated with a layer of silicon dioxide. Holes are cut through the silicon dioxide to make contact with the *n*-type blocks. Metal is deposited through the holes to form drain and source terminals, and on the surface area between drain and source, a metal plate is deposited. This plate, as will be seen, can function as a gate.

Consider the situation when the drain is made positive with respect to the source and no potential is applied to the gate. The two *n*-blocks and the *p*-type substrate form back-to-back *pn*-junctions connected by the resistance of the *p*-type material [Fig. 8-15(b)]. Both junctions cannot be forward biased at the same time, so only an extremely small drain current (i.e., a reverse leakage current) flows. If the *p*-type substrate is now connected to the source terminal, there is zero voltage across the source–substrate junction, and the drain–substrate junction remains reverse biased. When the gate is made positive with respect to the source and the substrate, negative (minority) charge carriers within the substrate are attracted to the (positive) gate. These charge carriers (electrons) accumulate close to the surface of the substrate, as illustrated in Fig. 8-15(c). As the gate potential is increased, more and more electrons accumulate under the gate. These electrons cannot flow across the silicon dioxide to the gate, so they accumulate at the substrate surface just below the gate. The minority charge carriers constitute an *n*-type channel stretching from drain to source. Thus, a drain current flows and its magnitude depends upon the channel resistance, which in turn depends upon the number of charge carriers attracted to the positive gate. The gate potential controls the drain current. Since the conductivity of the channel is *enhanced* by the

positive bias on the gate, the device is known as an *enhancement mode* MOSFET.

Typical drain and transfer characteristics for an enhancement mode MOSFET are shown in Fig. 8-16. Note that the drain current increases with positively increasing gate–source bias voltage. Because the gate of the MOSFET is insulated from the channel, there is no leakage current involved. This gives the device a very high input resistance, in some cases $10^{15}\ \Omega$ or greater. Transconductance values for MOSFETs typically range from 1000 μS to 2000 μS, i.e., from 1 to 2 mA/V.

Two symbols for the enhancement mode *n*-channel MOSFET are shown in Fig. 8-17. In each case, the fact that the device has an insulated gate is indicated by the gate not making direct contact with the channel. In each case the arrowhead is shown pointing from the *p*-type substate toward the *n*-type channel. One symbol shows the source and substrate internally connected, while the other symbol shows the substrate connection brought out separately from the source. The line representing the channel is broken into three sections to show that the channel does not exist until a gate voltage is applied, i.e., to show that the device operates in the *enhancement mode*.

A *p*-channel enhancement mode MOSFET is constructed by starting with an *n*-type substrate and diffusing *p*-type drain and source blocks. All

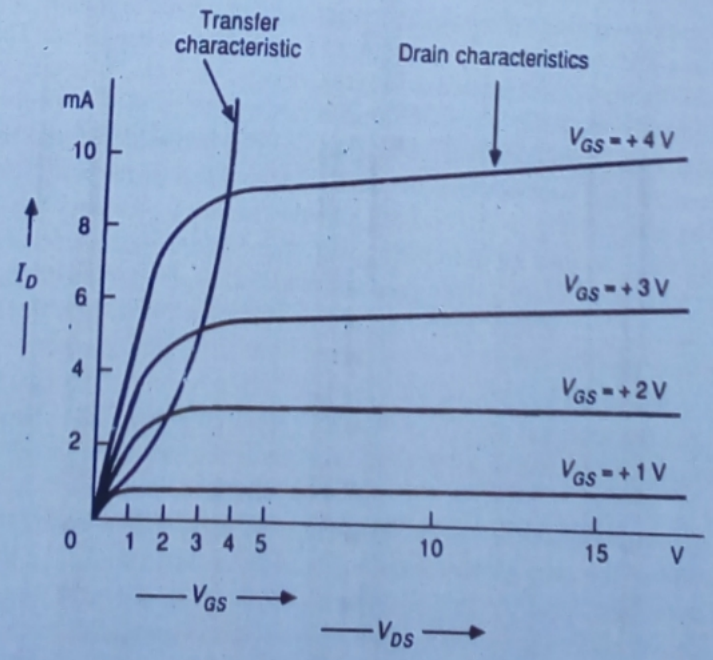


Figure 8-16 Drain and transfer characteristics for an *n*-channel enhancement-mode MOSFET. Progressively more positive levels of V_{GS} are required to increase the level of I_D.

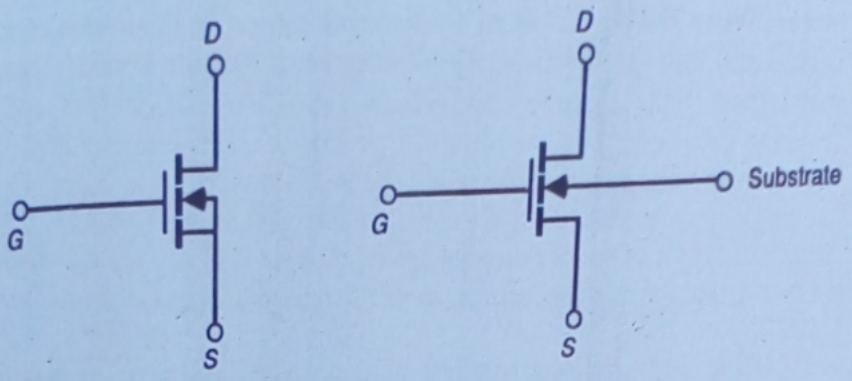
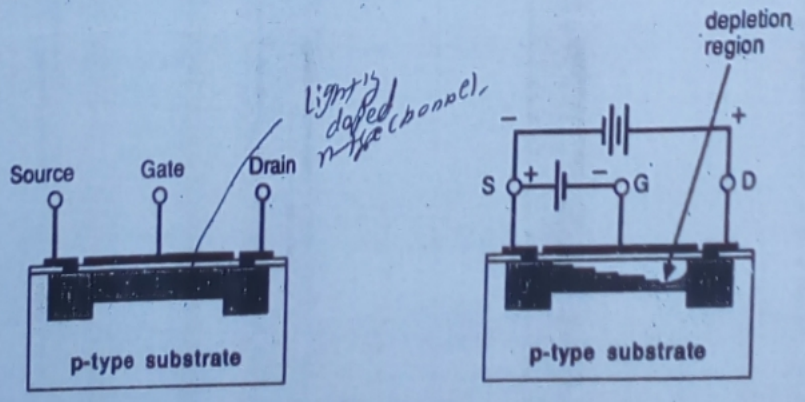


Figure 8-17 Circuit symbols for *n*-channel enhancement MOSFET. The gate bar is separated from the channel to show that there is no direct connection between them. The channel line is broken to indicate that no channel exists until an appropriate bias is applied.

voltage and current polarities are then the reverse of those for the *n*-channel device, and the direction of the arrowhead is reversed in the circuit symbol.

Depletion-Enhancement MOSFET

Consider the device illustrated in Fig. 8-18(a). The construction is the same as that for the enhancement mode MOSFET, except that a lightly doped *n*-type channel has been introduced between the two heavily doped source and drain



(a) n-channel depletion-enhancement MOSFET with no gate bias

(b) Depletion mode operation

Figure 8-18 The *n*-channel depletion-enhancement MOSFET is similar to the enhancement device, except that an *n*-type channel is included when the device is fabricated. The channel resistance may be increased or decreased by appropriate gate–source bias voltages.

blocks. When the drain is made positive with respect to the source, a drain current will flow, even with zero gate potential. If the gate is made negative with respect to the substrate, some of the negative charge carriers are repelled from the gate and driven out of the *n*-type channel. This creates a depletion region in the channel and causes the channel resistance to increase. Drain current is decreased, and the effect is similar to that in the *n*-channel JFET. Since the action of the negative voltage on the gate is to deplete the channel of free *n*-type charge carriers, the device is referred to as a *depletion-mode* MOSFET.

If the drain characteristics are plotted for various levels of negative gate–source voltage, the curves obtained are very similar to those of an *n*-channel JFET. Now consider what happens if the gate is made positive with respect to the substrate. Additional *n*-type charge carriers are attracted from the *p*-type substrate into the channel, so the channel resistance decreases. Therefore, the depletion-mode MOSFET is capable of operating in the enhancement mode also. The resultant characteristics are shown in Fig. 8-19.

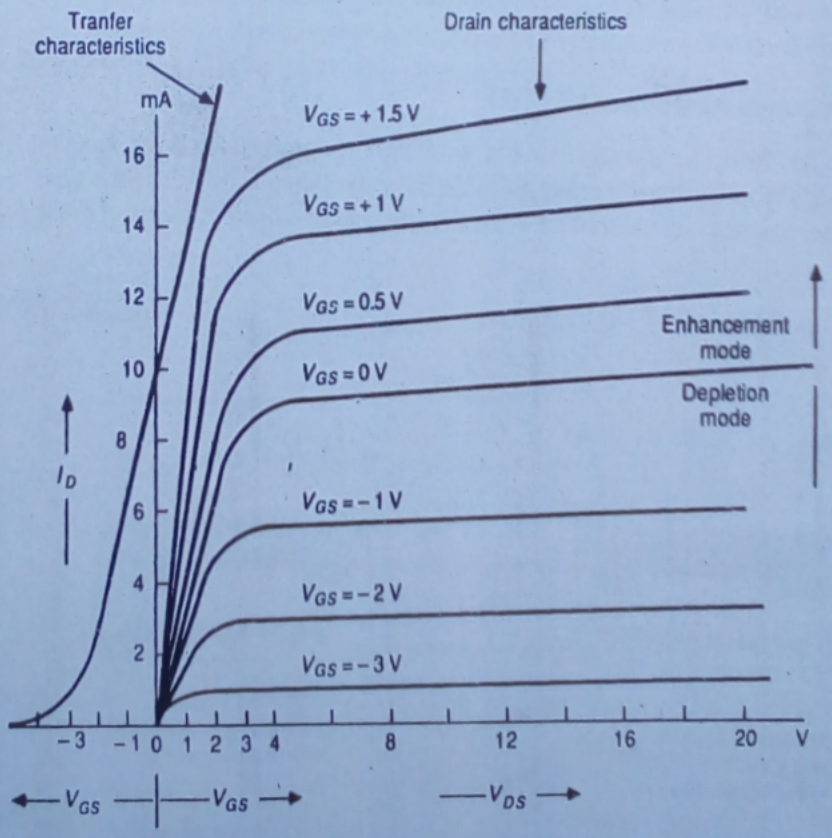


Figure 8-19 Drain and transfer characteristics for *n*-channel depletion-enhancement MOSFET. Drain current flows when $V_{GS} = 0$, and I_D may be increased or decreased by application of positive or negative levels of V_{GS}.